Customer No.: 31561
Application No.: 10/064,881
Docket No.: 9641-US-PA

AMENDMENTS

In The Specification

Please amend paragraph [0033] as follows:

[0033] Generally speaking, the clocks CLK2A and CLK2B require only the same frequency of the frame or the first clock CLK1, while synchronism is not a criterion. For example, the image data Vdata is output at the clock CLK2 to control the light-emitting device of the display 128. At clock CLK2B, a [[~~discharged~~]]discharging negative voltage corresponding to the current frame is output. The [[~~discharged~~]]discharging negative voltage is a kind of reset signal that allows the driver transistor 102 in Figure 1 to be switched off, such that the threshold value of the driver transistor 102 returns to the initial value. The clocks CLK2A and CLK2B are interchangeable. The following design provides a further description.

Please amend paragraph [0034] as follows:

[0034] The output control unit 202 includes a switch 208, for example, and can obtain the image data from the buffer memory unit. The output control unit 202 can also receive a [[~~discharged~~]]discharging negative voltage. The [[~~discharged~~]]discharging negative voltage can also be generated automatically at the output control unit 202. The output control unit 202 outputs the image data 204 to the display 128 at the clock CLK2A and outputs a reset signal 206 to the display 128 at the clock CLK2B to reset each corresponding pixel of the threshold voltage

of the driver transistor. For Figure 1, the reset signal 206 is a [[~~discharged~~]]discharging negative voltage. The [[~~discharged~~]]discharging negative voltage 206 is input as Vdata to the transistor 100 which is switched on at the second clock CLK2. Therefore, the [[~~discharged~~]]discharging negative voltage 206 switches off the driver transistor 102. The switch between the image data 204 and the [[~~discharged~~]]discharging negative voltage 206 is controlled by the switch 208. However, the switch 208 is not the only method for controlling the switching state. In terms of switching method, it can be set up to output the image data 204 at the clock CLK2B and to output the [[~~discharged~~]]discharging negative voltage 206 at clock CLK2A.

Please amend paragraph [0036] as follows:

[0036] The present invention further provides a driving method for a light-emitting device as shown in Figure 7. In step 300, a video signal saves an image data into a buffer memory unit 124 with a speed of the first clock CLK1. The first clock CLK1 defines the clock of the frame such as 60Hz. In step 302, two clocks CLK2A and CLK2B are obtained by partition operation according to the second clock CLK2. The second clock CLK2 is a multiple of the first clock CLK1, for example. Preferably, the second clock CLK2 is double of the first clock CLK1. The frequencies of the two clocks CLK2A and CLK2B are the same as the first clock CLK1, while a delay exists between them. The delay is preferably ½ of the frame. In step 304, a frame image data 204 is output at the clock CLK2A. Meanwhile, a

[[~~discharged~~]]discharging negative voltage 206 is also output at the clock CLK2A. The image data 203 corresponding to the frame can also be output at the clock CLK2B, while the [[~~discharged~~]]discharging negative voltage 206 is output at the clock CLK2A.